What is claimed is:

1. A high voltage device, comprising:

an N-type drift region and a P-type drift region formed on a substrate;

a gate region defined at an intersection between the N and P-type drift region, the gate region having an oxide film deposited on an upper portion of the gate region and a gate electrode formed on the oxide film;

a source region being defined in one of the N and P-type drift regions, the source region having a first trench filled with a first polysilicon layer, a first high density diffusion layer formed on an upper portion of the first polysilicon layer and a source electrode formed on the high density diffusion layer; and

a drain region being defined in the other of the N and P-type drift regions, the drain region having a second high density diffusion layer formed on an upper portion of the drain region and a drain electrode formed on the second high density diffusion layer.

2. The high voltage device according to claim 1, further comprising:

a second polysilicon layer filling a second trench formed between the N and P-type drift regions of the gate region such that the oxide film is deposited in the second trench as well as the upper portion of the drift region corresponding to the drain region.

3. The high voltage device according to claim 1, wherein the first polysilicon is formed in the first trench such that a depth of the first trench is substantially equal to a depth of the one of the N and P-type drift region where the source region is defined.

4. The high voltage device according to claim 1, wherein the first trench is formed at the P-type drift region.

5. The high voltage device according to claim 4, wherein the first high density diffusion layer is an N^+ layer.

6. The high voltage device according to claim 5, wherein the second high density diffusion layer is an N^+ layer.

7. The high voltage device according to claim 5, further comprising:

a third high density diffusion layer in the source region adjacent to the first high density layer.

8. The high voltage device according to claim 7, wherein the third high density diffusion layer is a P^+ layer.

9. A high voltage device, comprising:

a substrate;

a first drift region and a second drift region formed in the substrate;

a gate electrode formed over a gate region, the gate region being defined over an intersection of said first and second drift regions such that said gate region includes a part of said first drift region and a part of said second drift region;

a first polysilicon layer filling a first trench formed in a source region, the source region being defined in said first drift region;

a first high density diffusion layer formed in an upper portion of the source region including a portion of the first polysilicon layer and a portion of the first drift region in between the first trench and the gate region; and

a second high density diffusion layer formed in a drain region, the drain region being defined in the second drift region.

10. The high voltage device of claim 9, wherein the first drift region is of P-type and the second drift region is of N-type.

11. The high voltage device of claim 9, wherein the first high density diffusion layer is of N^+ type.

12. The high voltage device of claim 11, wherein the second high density diffusion layer is of N^+ type.

13. The high voltage device of claim 9, further including:

a third high density diffusion layer formed in another portion of the source region adjacent to the first high density diffusion layer.

14. The high voltage device of claim 13, wherein the third high density diffusion layer is of P^+ type.

15. The high voltage device of claim 9, further including:

an oxide film formed in a second trench formed in the gate region, the oxide film also formed on an upper portion of the gate region in between the second trench and the drain region; and

a second polysilicon layer filling the second trench covering the oxide film formed within the second trench such that the gate electrode covers at least a portion of the second polysilicon layer and the oxide film on the upper portion of the gate region.

16. A method for forming a high voltage device, comprising:

forming a first drift region and a second drift region in a substrate;

forming a gate electrode over a gate region, the gate region being defined over an intersection of said first and second drift regions such that said gate region includes a part of said first drift region and a part of said second drift region;

forming a first trench in a source region, the source region being defined in said first drift region;

filling the first trench with a first polysilicon layer;

forming a first high density diffusion layer in an upper portion of the source region including a portion of the first polysilicon layer and a portion of the first drift region in between the first trench and the gate region; and

forming a second high density diffusion layer in a drain region, the drain region being defined in the second drift region.

17. The method of claim 16, wherein the first drift region is of P-type and the second drift region is of N-type.

18. The method of claim 16, wherein the first high density diffusion layer is of N^+ type.

19. The method of claim 18, wherein the second high density diffusion layer is also of N^+ type.

20. The method of claim 16, further forming a third high density diffusion layer in another portion of the source region adjacent to the first high density diffusion layer.

21. The method of claim 20, wherein the third high density diffusion layer is of P^+ type.

22. The method of claim 16, further including:

forming a second trench in the gate region,

forming an oxide film in the trench and on an upper portion of the gate region in between the second trench and the drain region; and

filling the second trench with a second polysilicon layer covering the oxide film formed within the second trench such that the gate electrode covers at least a portion of the second polysilicon layer and the oxide film on the upper portion of the gate region.